## REMARKS

Claims 16-30 are pending in the application. Claims 16, 19 and 24 are rejected. Claims 17, 18, 20-23 and 25-30 are objected to but would be allowable if placed into independent form. Applicant has amended claims 16 and 24 in order to better define over the prior art. Applicant also has amended claims 17, 20-22 and 25-29 in order to place them into independent form and secure their allowability.

### *Claim Rejections – 35 USC 102*

**Claims 16, 19 and 24 are rejected under 35 USC 102(e) as being anticipated by Eklund (6,392,575).** This rejection is traversed for at least the following reasons.

As a preliminary matter, independent claims 16 and 24 are directed to a semiconductor integrated circuit that has an analog/digital converting circuit for converting an analog image signal to a digital image signal. There is no teaching of a semiconductor circuit in Eklund, thereby precluding anticipation. Moreover, the Examiner admits that Eklund does not teach a conversion of an image signal, but asserts that the mention of a "communications" system at col. 1, lines 15-17 could include images. The Examiner's assertion does not support a rejection based on anticipation.

The present application explains in the Background section the unique problems that occur with the conversion of pixels in an analog image signal in a semiconductor circuit. In the absence of an express teaching of an image signal in a semiconductor, or an inherent feature of communications signals to include image signals, the rejection must be withdrawn and replaced by a rejection under 35 USC 103. Nonetheless, in the interest of advancing the prosecution of the application to issue, Applicants have modified the claims to more specifically tie the operation of the control circuit to a synchronization signal that corresponds to the analog image signal.

Turning next to the substance of the rejection, independent claim 16 is directed to a semiconductor integrated circuit comprising a plurality of analog/digital converting circuits operated in parallel for sequentially converting an analog image signal to a digital image signal and a multi-phase clock signal generating circuit for generating multi-phase clock signals to be

used for periodically operating said plurality of analog/digital converting circuits in a certain order. The claimed invention also includes a control circuit for controlling the multi-phase clock signal generating circuit to change at least one of a period and an order of operating the plurality of analog/digital converting circuits. Exemplary embodiments of the subject matter of this aspect of the invention are presented with respect to Figs. 1, 4, 6 and 8, where plural imaging ADCs 11 are switched according to multi-phase signals from multi-phase generating clock signal circuits 12, 32, 52 and 71, respectively, under operation of respective control signal generating circuits 20, 40, 60 and 80. As noted in Figs. 4 and 8, a VSYNC signal (or HSYNC signal as noted at pages 12-13) can be input to the sampling control signal generating circuit 40, 80 to control the output selection process. The claim has been amended to specify that the control circuit is responsive to at lease a synchronization signal which corresponds to the analog image signal.

Independent claim 24 is also directed to a semiconductor integrated circuit having an analog/digital converting circuit that sequentially switches between a plurality of circuit elements and a first control circuit for controlling the analog/digital converting circuit to periodically arrange the plurality of circuit elements in a certain order. The claimed invention also includes a second control circuit for controlling the first control circuit to change at least one of a period and an order of arranging the plurality of circuit elements. An exemplary embodiment of the subject matter of this aspect of the invention is presented with respect to Fig. 11, where a single imaging ADC has plural elements 91 that are switched according to multi-phase signals from control circuit 93 under operation of control signal generating circuit 100. The claim has been amended to expressly state that the control circuit is responsive to at lease a synchronization signal which corresponds to the analog image signal.

**Eklund**

The Examiner points to Fig. 4 of Eklund for an illustration of a parallel ADC device that has multiple A/D channel circuits 13, wherein the several circuits receive a common input signal via respective sample and hold circuits 11 and provide their outputs to a multiplexer 17 for providing a flow of digital words at the same rate as the sampling rate. As explained at col. 3, line 26-col. 4, line 19, each output digital word represents the input analog signal at a

predetermined period, and subject to a delay inherent in the processing of the input signal sample. While there are five parallel paths shown, fewer than all of them are operational at any given time, and the timing of their selection is determined by a timing control circuit 15.

Details of the timing control circuit 15 are provided in Fig. 6, and explained at col. 4, line 20-col. 5, line 27. The process of selecting the next channel for processing is based on an identification of the working channels, an identification of one of the working channels in an intermediate register 39, and the designation of that channel as an idle channel in register 31. A random number generator 21 outputs a sequence of 1 and 0 values that determine whether a number of a working channel or the idle channel is provided to a selector 37. The selector 37 operates cyclically in response to clock pulses from clock signal generator 23, and does not respond to the content of the input signal itself. The result is a correction of jitter and gain errors, which are caused by differences among the several circuits, based on a distribution of errors.

Notwithstanding these teachings, a basis for distinguishing the invention of claims 16 and 24 would lie in Applicant's further definition of the control circuit as having the function of controlling the multi-phase clock signal generating circuit to change at least one of a period and an order of operating said plurality of analog/digital converting circuits in response to at least a synchronization signal which corresponds to the analog image signal.. This feature is not taught in the prior art, thus making claims 16 and 24 patentable.

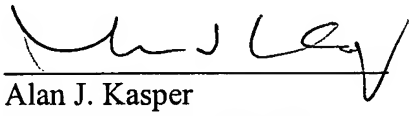
***Allowable Subject Matter***

The Examiner finds that claims 17-23 and 25-30 to be patentable if placed into independent form. Applicant has amended 17, 20-22 and 25-29 in order to place these claims into independent form and to secure their allowability, as well as that of the claims that depend from them.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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23373
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Date: May 20, 2005